Sponsoring societies

In cooperation with

Premium contributors

Industrial/Academic contributors
GENERAL INFORMATION

WELCOME TO GRENOBLE
The City of Grenoble is a unique natural environment, an economic, technological and university network that encourages innovation, great artistic and cultural wealth: Grenoble – the choice of excellence: To get more information about Grenoble see http://en.wikipedia.org/wiki/Grenoble

The Rhône-Alpes region is known for its concentrated high-level expertise in the Embedded Systems field due to the effective transfer of technology between Industry, Research, Education. A leading industrial sector with more than 2,000 companies generating over 63,000 industrial jobs in the Region and a turnover of € 11 billion.

The region boasts a major concentration of high-level international research and employs over 6,000 researchers.

More than 30,000 students receive specialised training and education in every Embedded Systems field.

Embedded System industry in Rhône-Alpes directly accounts for over 60000 jobs (and indirectly over three times as much) 35000 of which in Grenoble itself:
- 11000 in electronics,
- 11000 in Information Technology,
- 7000 in micro-electronics
- and 6000 in software development

Grenoble itself boasts one of the largest Scientific Communities in France, forming the largest centre for research after Paris, with a training potential of 61000 students.

ACCESSING GRENOBLE
Grenoble is 145 km away from Geneva (Switzerland) and 247 km away from Turin. Within France, the city lies 106 km away from Lyon, 149km from Chamonix.

It is accessible by 2 airports:
- Lyon Saint-Exupéry Airport (45 minutes from Grenoble downtown) connected to all over the world
- Geneva Cointrin International Airport (90 minutes from from Grenoble downtown), connected to all over the world

There are several options to travel to and from the Lyon Saint-Exupéry airport. The easiest and cheapest is by bus (1 hour and 5 minutes, 20 euros one way, departing each hour), which arrives directly at Grenoble’s railway station. Taking a taxi from the airport to Grenoble’s railway station costs around 120 euros; this trip should take around 1 hour depending on traffic.

COLOQUED EVENT

Embedded Linux Conference Europe (ELC-E) 2009

Come and join us!

ELC-E is a meeting point of the international open source software developers for embedded systems together with other community people. It will be held during ESWEEK in the World Trade Center (Grenoble, France) on October 15th and 16th, 2009. Through the variety of sessions, Bofs, tutorials, technical showcases and evening reception we will exchange knowledge of open source software technologies. Come join us and be inspired by technical ideas on the evolution of Linux and related software for embedded systems, and at the same time be connected with your counterparts in this industry.

ELC-E is unique in that it draws many core developers from around the world who are enthusiastic about building Linux-based software systems for small footprint environments. Most of these developers are engaged in development projects of Linux embedded products. At the ELC-E you will experience the cutting edge of the Linux evolution.

Who should join?
Anyone interested in embedded system software technologies are encouraged to join us at the ELC-E. Not only the actual developers but also the managers and media will find many advancements being discussed for the future of the software design. Please visit our home page for the details.

http://www.embeddedlinuxconference.com

Conference highlights
Keynote speakers Jon Masters and Philippe Gerum will talk about recent trends in Linux development including the state of real-time Linux - from two isolated kernels to a single pervasive real-time system. Also Gilad Ben-Yossef will present a talk, completing the main writers of the well-known book “Building Embedded Linux Systems”. Another famous Linux author, Alessandro Rubini, will talk about the use of the fast IRQ in ARM-Linux, and many more topics will be addressed ranging from embedded Linux distributions and build systems to application frameworks for rich UI.

Please see the session list at the ELC-E homepage for a complete overview.

Consumer Electronics Linux Forum (CELF)
Main sponsor of the event is the Consumer Electronics Linux Forum (CELF). CELF is an international open source software development community established in 2003. It is a forum of like-minded software engineers dedicated to the development and enhancement of Linux-based embedded devices through the irreplaceable resource of shared knowledge. These engineers bring their ideas and finest skills to such missions as decreasing system size, startup/shutdown time, and power consumption; improving compatibility to various CPU architectures, and developing middleware

http://celinuxforum.org/

CE Linux Forum
3855 SW 153rd Drive
Beaverton, Oregon 97006 USA
Telephone: +1.503.619.0855
Facsimile: +1.503.644.6708
E-mail: office@celinuxforum.org
Welcome to the 1st edition of the Embedded Systems Exhibition and find out some of the most innovative companies of the Grenoble area! 30 exhibitors will show you their outstanding know-how and technological roadmap. We expect more than 700 visitors on the exhibition.

If you wish to exhibit on ESE, go to www.minalogic.com

Special fee for early booking (20/09/2009)

This event is organized by Minalogic, global competitive cluster in micro nanotechnologies and embedded software. Located in Grenoble, France, the cluster channels in a single physical location a range of highly-specialized skills and resources from knowledge creation to the development and production of intelligent miniaturized services for industry.

It is also possible to arrive to Grenoble by train with SNCF, which has train services from all the major cities in France and in Europe. The conference center and Novotel hotel are just at two minutes walking distance from Grenoble’s railway station.

**HOTEL INFORMATION**
The conference hotel is Novotel. We have compiled a pre-selection of hotels with special prices for ESWeek attendees.

<table>
<thead>
<tr>
<th>Hotel Address</th>
<th>Phone +33.(0)</th>
<th>Fax +33.(0)</th>
<th>ESWeek rate Single room</th>
<th>Website</th>
</tr>
</thead>
<tbody>
<tr>
<td>*** Grand Hôtel MERCURE Président 11, rue Général Mangin 38100 Grenoble 04 76562656 04 76562682 149 €</td>
<td><a href="http://www.mercure.com">www.mercure.com</a> hotel web code: 2947</td>
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<tr>
<td>*** NOVOTEL Grenoble CENTRE 7, place Robert Schuman 38000 Grenoble 04 76708484 04 76708420 143 €</td>
<td><a href="http://www.novotel.com">www.novotel.com</a> hotel web code: 1624</td>
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<tr>
<td>*** Hôtel MERCURE Alpotel 12, Bd Maréchal Joffre 38000 Grenoble 04 76878841 04 76475852 128 €</td>
<td><a href="http://www.mercure.com">www.mercure.com</a> hotel web code: 0652</td>
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Other Hotels in Grenoble and its neighbourhood can be reserved with the Tourist office of Grenoble. You will find a wide selection of hotels and the promotions for successful stays:

www.grenoble-resatourisme.com   Tel: +33(0)4.56.52.38.38

Of course, you can book directly your hotel via any web broker.

More information also available on http://www.esweek.org
Grenoble Welcome Reception to ESWeek, ELC-E & ESE at WTC
Wednesday, Oct. 14th 2009 – 19:45

World Trade Center
Grenoble
Place Robert-Schuman
38025 Grenoble
Tel.: +33 (0)4 76 28 28 40
Gala Banquet
at Chavant Restaurant
Tuesday, Oct. 13th 2009 - 20:00

5 Emile Chavant,
38320 Bresson
Tel: +33 (0)4 76 25 25 38

Keynote: Monday October 12, 2009

Automotive: Driving Embedded Systems On Wheels
Over the last few decades the amount of electronics in cars has grown rapidly, and with it the amount of embedded software. This is however just the beginning, we are entering a new era driven by trends towards green and efficient driving, safety, electrical vehicles and connected cars through “intelligent traffic systems”. Not only will this drive even more electronic systems in cars, it will also create a plethora of connected embedded systems on many levels in cars, between cars and their environment, and between cars. This will offer great opportunities to create the green connected car of the future, and it will also create many challenges in the areas of safety and security, energy efficiency and managing complexity.

Cars will have many networked nodes and “Drive by -X” trends will require systems that are deterministic in behavior. Real time requirements and the need for resilient systems will also influence future car architectures. The car as part of a continuous driving network will influence car architectures as well as human interaction with the car and open up possibilities of many new services.

In this talk we will explore these trends and some consequences for embedded system design.

Ir. Carol de Vries,
Vice president R&D Business Unit Automotive NXP Semiconductors
Carol de Vries is currently responsible for all R&D activities in the Automotive Business Unit of NXP Semiconductors, active in car infotainment, car networking, car access, telematics and intelligent traffic systems. Prior to joining NXP, Carol worked for Philips Electronics in different functions. Carol started his career in Philips Research on semiconductors. Later he became responsible for the CCD imaging activities, and served in a number of other management positions in the fields of passive integration, power modules, hard disk recording, consumer networking and LCD TV. Returning to Semiconductors Carol first focused on SoC process and IP development from 90nm to 45nm nodes before assuming his current position.
Keynote: Tuesday October 13, 2009

The Time-Triggered Architecture

The time-triggered architecture (TTA) establishes a framework for the construction of distributed embedded computing systems. The following three challenges have driven the development of this architecture: complexity management, robustness and energy efficiency. The TTA lifts the design process to a higher level of abstraction by introducing nearly autonomous hardware/software components as the basic building blocks. The components communicate exclusively by the exchange of messages. The TTA provides a global time-base to all components and uses this time to ensure the temporal validity of the real-time data and the timely response of the computer system. The TTA provides fault-containment and error containment as an architectural service, such that fault-tolerant systems can be built without undue effort. After short discussion of generic embedded system requirements, this talk will focus on the architectural principles and the services of the time-triggered architecture.

Prof. Dr. Hermann Kopetz
Vienna University of Technology

Hermann Kopetz received his PhD in physics “sub auspiciis praesidentis” from the University of Vienna, Austria in 1968. After eight years industry he accepted in 1979 an appointment as a Professor for Computer Process Control at the Technical University of West-Berlin. Since 1982 he is Professor for Software Engineering and Real-Time Systems at the Vienna University of Technology. Dr. Kopetz is a “Fellow of the IEEE” and was the Chairman of the IFIP WG 10.4 on Dependable Computing and Fault-Tolerance from 1996 to 1998. In 1998 he was elected to become a full member of the Austrian Academy of Science and in 2007 he received the degree of Dr. h.c. from the University Paul Sabatier in Toulouse. Dr Kopetz has published a widely used textbook on Real-Time Systems and more than 150 papers on the topic of dependable embedded systems. He is the inventor of the time-triggered technology, which recently has been selected by NASA for deployment in the ORION program. He holds more than twenty patents. Dr. Kopetz received the IEEE Computer Society 2003 Technical Achievement Award with the citation: For outstanding contributions to the field of safety-critical real-time computing. Since 2007 Dr. Kopetz is a member of the prestigious Information Society Technology Advisory Group (ISTAG) of the EU Commission in Brussels, advising the Commission on the future trends in the ICT area.

Committee Dinner
at Chez Pignol
Monday, Oct.12th 2009 – 19:30

Pignol Sainte Cécile
Rue Dominique Villars
38000 Grenoble
Tel : +33 (0)4 76 24 85 85
Welcome Reception at WTC  
Sunday, Oct. 11th 2009 – 19:00

World Trade Center  
Grenoble  
Place Robert-Schuman  
38025 Grenoble  
Tel. : +33 (0)4 76 28 28 40

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The end of embedded software?
The term “embedded software” suggests software that is isolated and contained inside hardware components. Increasingly, realizing the maximum value in systems depends on taking the opposite view, where software is an open, extensible, connected virtual environment connected to the physical world by hardware. In this talk we will discuss how companies that take this view are changing industries and look at the methods and tools they use to develop software.

**Dr. Martin Nally,**  
**Chief Technical Officer, IBM Rational Software**  
Martin Nally is an IBM Fellow and currently the Chief Technology Officer for the Rational Software division of IBM. Martin joined IBM in 1990 with 10 years’ prior industry experience. He has held several architecture and development positions in IBM including lead architect and developer for IBM VisualAge/Smalltalk and VisualAge/Java. Martin was one of a team of three that launched the IBM project that later became the Eclipse framework and he led the architecture, design and development of WebSphere Studio, IBM’s flagship Eclipse-based developer tool-suite that later evolved into Rational Application Developer.
| Session 8A: Performance Analysis and Optimization for Heterogeneous Multiprocessor Systems | Session 8B: Architecture and Optimization of NoC | Session 2: Key Industrial Computing Platforms to Enable Embedded Systems
|
|----------------------------------|---------------------|-----------------------|
| Session chair: Jurgen Teich     | Session chair: Kees Goossens | Organizer: Luca Benini  
|
|
| Yu Wang, Jiaxiu Sheng, Shenxi Zhang Yang | Yue Qian, Zhonghai Lu and Wenhua Dou | Naoki Nishii  
|
| 7.2 A Caching and Reconfigurability Algorithm for On-Fly Reconfiguration. | 8.2 Bottom-Up Performance Analysis Considering Time Slice and Dynamic Scheduling at System Level. | 2.2 ARM MPCore Technology for Scalable, Low-Power Embedded Computing.  
|
| Junseok Park, Hyeongeun Lee, Suungmin Kim, HyoKyung Bahn and Kern Koh | Alexander Viehl, Michael Pressler and Oliver Brinnmarsh | John Goodacre  
|
| 7.3 Towards Scalable Reliability Frameworks For Error Prone CPMs. | 8.3 A Recursive Approach to End-To-End Path Latency Analysis in Heterogeneous Multiprocessor Systems. | 2.3 The X-GOLD SDR2x Platform for Multi-Standard Baseband Computing.  
|
| Joseph Sloan And Rakesh Kumar | Simon Schliecker and Rolf Ernst | Ulrich Ramachers  
|
|
| Yongjun Park, Hyunchul Park and Scott Mahlke | Antonino Tumeo, Marco Branca, Lorenzo Camerini, Christian Piatto, Fabrizio Ferrandi, Pier Luca Lanzoni and Donatella Scito | Fabien Clermidy  
<p>|
|
| Mark Lau, Keck-Voon Ling and Yung Chung Chu | Mark Lau, Keck-Voon Ling and Yung Chung Chu | Matthias Bo, Stuart, Mikkel Bystrop Stensgaard and Jens Sparso |</p>
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<tr>
<th>Session 7A: Emerging Techniques</th>
<th>Session chair: Robert Walker</th>
<th>Session co-chair: Wolfgang Ecker</th>
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</thead>
<tbody>
<tr>
<td>7.1 A Scalable Parallel H.264 Decoder on the IBM Cell Broadband Engine Architecture</td>
<td>Michael A. Baker, Pravin Dalale, Karam S. Chatha and Sarma B. K. Vrudhula</td>
<td></td>
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<tr>
<td>7.2 FlexRay Schedule Optimization of the Static Segment</td>
<td>Martin Lukasiewycz, Michael Glas, Paul Milbredt and Jurgen Teich</td>
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<tr>
<td>7.3 Improving Application Launch Times with Hybrid Disks</td>
<td>Yongsoo Joo, Youngjin Cho, Kyungsoo Lee and Naehyuck Chang</td>
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<tr>
<th>Session 7.B: Exploring the Hardware Software Boundaries for MPSoC Design</th>
<th>Session chair: Sungyoo Yoo</th>
<th>Session co-chair: Falrien Clermidy</th>
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</thead>
<tbody>
<tr>
<td>7.1 A Tuneable Software Cache Coherence Protocol for Heterogeneous MPSoCs</td>
<td>Frank Ophelders, Marco Bekooij and Henk Corporaal</td>
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<tr>
<td>7.2 Building Heterogeneous Reconfigurable Systems With A Hardware Microkernel</td>
<td>Jason Agron and David Andrews</td>
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<tr>
<td>7.3 Native MPSoC Co-Simulation Environment for Software Performance Estimation</td>
<td>Patrice Gerin, Mian Muhammad Hamayun and Frederic Petrot</td>
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<tr>
<th>Session 8: Time Predictability and Memory Management</th>
<th>Session chair: Reinhard Wilhelm</th>
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<tbody>
<tr>
<td>8.1 Cache-Aware Scheduling and Analysis for Multicores</td>
<td>Nan Guan, Martin Stigge, Wang Yi and Ge Yu</td>
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<tr>
<td>8.2 Probabilistic Modeling of Data Cache Behavior</td>
<td>Vinayak Puranik, Tulika Mitra and Y. N. Srikant</td>
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<tr>
<td>8.3 Implementing Time-Predictable Load and Store Instructions</td>
<td>Jack Whitham and Neil Audsley</td>
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<tr>
<td>8.4 Dataflow Models for Shared Memory Access</td>
<td>Jan Staschulat and Marco Wilhelm</td>
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<tr>
<th>Session 1: Key Embedded System End Users</th>
<th>Session chair: Jan Madsen</th>
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<tbody>
<tr>
<td>1.1 Mobile Computing Platform, a Dream?</td>
<td>Frank Ghenassia</td>
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<tr>
<td>1.2 Multimedia on Multi-Processors = Multi Challenges?</td>
<td>Pierre Paulin</td>
</tr>
<tr>
<td>1.3 New challenges in engineering and computing for embedded critical systems</td>
<td>Eric Lenormand</td>
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<tr>
<td>1.4 Eating your own dog food – i.e. what happens when you start using your own tools and processors in earnest to build systems</td>
<td>Chris Rowen</td>
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<tr>
<th>INDUSTRIAL DAY</th>
<th>Session legend</th>
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<tr>
<td>POSTER SESSION @ 12:00</td>
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<td>MONDAY OCT. 12</td>
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</table>
### Session 6: Microfluidics, Worst-Case Execution Time, and Cache Optimization

**Session chair:** Tulika Mitra  
**Session co-chair:** Tony Givargis

<table>
<thead>
<tr>
<th>Time</th>
<th>Speaker(s)</th>
<th>Title</th>
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<tbody>
<tr>
<td>14:00</td>
<td>Jin Ouyang, Raghuveer Raghavendra, Sibin Mohan, Tao Zhang, Yuan Xie and Frank Mueller</td>
<td><strong>6.1 CheckerCore: Enhancing An FPGA Soft Core To Capture Worst-Case Execution Times.</strong></td>
</tr>
<tr>
<td>14:30</td>
<td>Kapil Anand and Rajeev Barua</td>
<td><strong>6.2 Instruction Cache Locking Inside A Binary Rewriter.</strong></td>
</tr>
<tr>
<td>15:00</td>
<td>Elena Maftei, Paul Pop and Jan Madsen</td>
<td><strong>6.3 Tabu Search-Based Synthesis Of Dynamically Reconfigurable Digital Microfluidic Biochips.</strong></td>
</tr>
<tr>
<td>15:30</td>
<td>Partha S Roop, Sidharta Andalam, Simon Yuan and Claus Traulsen</td>
<td><strong>6.4 Tight WRCT Analysis Of Synchronous C Programs.</strong></td>
</tr>
</tbody>
</table>

### Session 6A: System Level Reconfiguration and Architecture Optimization

**Session chair:** Christian Haubelt  
**Session co-chair:** Oliver Bringwaun

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<thead>
<tr>
<th>Time</th>
<th>Speaker(s)</th>
<th>Title</th>
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<tbody>
<tr>
<td>14:00</td>
<td>Vincenzo Rana, Srinivasan Murali, David Atienza, Marco D. Santambrogio, Luca Benini and Donatella Sciuto</td>
<td><strong>6.1 Minimization of the reconfiguration latency for the mapping of applications on FPGA-based systems.</strong></td>
</tr>
<tr>
<td>14:30</td>
<td>Lars Bauer, Muhammad Shafique and Jorg Henkel</td>
<td><strong>6.2 MinDeg: A Performance-guided Replacement Policy for Run-time Reconfigurable Accelerators.</strong></td>
</tr>
<tr>
<td>15:00</td>
<td>Daniel Schwartz-Narbonne, Carven Chan, Yogesh Mahajan and Sharad Malik</td>
<td><strong>6.3 Supporting RTL Flow Compatibilization in a Microarchitecture-Level Design Environment.</strong></td>
</tr>
</tbody>
</table>

### Session 6: Multicore, Parallel Implementations

**Session chair:** Bengt Jonsson

<table>
<thead>
<tr>
<th>Time</th>
<th>Speaker(s)</th>
<th>Title</th>
</tr>
</thead>
<tbody>
<tr>
<td>14:00</td>
<td>Yuanrui Zhang, Mahmut Kandemir, Nikos Pitsianis and Xiaobai Sun</td>
<td><strong>6.1 Exploring Parallelization Strategies for NUFFT Data Translation.</strong></td>
</tr>
<tr>
<td>14:30</td>
<td>Meng-Huan Wu, Cheng-Yang Fu, Peng-Chih Wang and Ren-Song Tsay</td>
<td><strong>6.2 An Effective Synchronization Approach for Fast and Accurate Multi-core Instruction-set Simulation.</strong></td>
</tr>
<tr>
<td>15:00</td>
<td>Rebecca Collins and Luca Carloni</td>
<td><strong>6.3 Flexible Filters: Load Balancing Through Backpressure for Stream Programs.</strong></td>
</tr>
</tbody>
</table>
Session 5: Pervasive Parallelism
Session chair: Jiang Xu
Session co-chair: Yuan Xie

5.1 A Buffer Replacement Algorithm
Jinho Seol, Hyotaek Shim, Jaegeuk Kim and Seungryoul Maeng

5.2 Exposing Non-Standard Architectures to Embedded Software Using Compile-Time Virtualisation.
Ian Gray and Neil Audsley

5.3 Occam: A Platform For Developing Adaptable Multicore Applications.
Dan Fay, Li Shang and Dirk Grunwald

5.4 Parallel, Hardware-Supported Interrupt Handling in the CiAO Operating System on the Tricore Microcontroller.
Fabian Scheler, Wanja Hofer, Benjamin Oechslein, Rudi Pfister, Daniel Lohmann and Wolfgang Schröder-Preikschat

Session 5A: Embedded System Optimization Across Memory Hierarchy
Session chair: Jason Xue
Session co-chair: Cathy Gebotys

5.1 Squashing Microcode Stores to Size in Embedded Systems while Delivering Rapid Microcode Accesses.
Chengmo Yang, Mingjing Chen and Alex Orailoglu

5.2 Stack Oriented Data Cache Filtering.
Rodrigo Gonzalez-Alberquilla, Fernando Castro, Luis Pinuel and Francisco Tirado

5.3 ILP Optimal Scheduling for Multi-Module Memory.
Meikang Qiu, Lei Zhang and Edwin Sha

Session 5B: Efficient Techniques for Architecture Simulation
Session chair: Rolf Ernst
Session co-chair: Donatella Sciuto

5.1 Cycle Count Accurate Memory Modeling in System Level Design.
Yi-Len Lo, Mao-Lin Li and Ren-Song Tsay

Mohammad Shihabul Haque, Andhi Janapsatya and Sri Parameswaran

5.3 TotalProf: A Fast and Accurate Retargetable Source Code Profiler.
Lei Gao, Jia Huang, Jianjiang Ceng, Rainer Leupers, Gerd Ascheid and Heinrich Meyr

5.4 Using Continuous Statistical Machine Learning to Enable High-Speed Performance Prediction in Hybrid Instruction-/Cycle-Accurate Instruction Set Simulators.
Daniel Powell and Bjorn Franke

Session 5: Scheduling
Session chair: Luca Carloni

5.1 Clock-driven distributed real-time implementation of endochronous synchronous programs.
Dumitru Potop-Butucaru, Robert de Simone, Yves Sorel and Jean-Pierre Talpin

5.2 A family of compatible synchronisation protocols based on SIRAP.
Moris Behnam, Thomas Nolte and Reinder Bril

5.3 Towards a Time-Triggered Schedule Calculation Tool to Support Model-Based Embedded Software Design.
Joseph Porter, Gabor Karsai and Janos Sztipanovits

5.4 Monotonicity and Run-Time Scheduling.
Maarten Wiggers, Marco Beelen and Gerard Smit

EMSOFTCODES + ISSS
October 13, Tuesday 14:00 - 16:00
Session 4: Architectural Optimizations
Session chair: Oliver Bringmann
Session co-chair: Karam Chatha

Peter Yiannacouras, J. Gregory Steffan and Jonathan Rose

4.2 Fine-Grained Parallel Application Specific Computing for RNA Secondary Structure Prediction using SCFGs on FPGA.
Fei Xia and Yong Dou

4.3 Reducing Impact Of Cache Miss Stalls in Embedded Systems by Extracting Guaranteed Independent Instructions.
Garo Bournoutian and Alex Orailoglu

Alexander Fell, Mythri Alle, Keshavan Vadarajan, Prasenjit Biswas, Saptarsi Das, Jugantor Chetia, S.K. Nandy and Ranjani Narayan

Session 4A: Power-Aware Design Methodology
Session chair: Ann Gordon-Ross
Session co-chair: Naehynck Chang

Alireza Ejlali, Bashir Al-Hashimi and Petru Eles

4.2 Efficient Dynamic Voltage/Frequency Scaling through Algorithmic Loop Transformation.
Mohammad Ali Ghodrat and Tony Givargis

4.3 Energy-Efficiency for Multiframe Real-Time Tasks on a Dynamic Voltage Scaling Processor.
Chuan-Yue Yang, Jian-Jia Chen and Tei-Wei Kuo

Session 4B: Synthesis and Analysis for Variation and Reliability
Session chair: Robert Dick
Session co-chair: Sudeep Pasricha

4.1 A Variation-Tolerant Scheduler for Better Than Worst-Case Behavioral Synthesis.
Kai Lampka, Simon Perathoner and Lothar Thiele

4.2 Exploiting Data Redundancy in Reliability-Aware Embedded System Design.
Bjorn Sander, Jurgen Schnerr and Oliver Bringmann

4.3 ESL Power Analysis of Embedded Processors for Temperature and Reliability Estimations.
Bjorn Sander, Jurgen Schnerr and Oliver Bringmann

Session 4: Timing and performance analysis
Session chair: S. Ramesh

Kai Lampka, Simon Perathoner and Lothar Thiele

4.2 Serving embedded content via Web applications: model, design and implementation.
Simon Duquennoy, Gilles Grimaud and Jean-Jacques Vandewalle

4.3 Modular Performance Analysis of Cyclic Dataflow Graphs.
Lothar Thiele and Nikolay Stoimenov

4.4 Symbolic State Traversal for WCET Analysis.
Stephan Wilhelm and Bjoern Wachter
SESSION LEGEND

SESSION 1: SPECIAL SESSION I

1.1 Sustaining Moore’s Law in Embedded Computing through Probabilistic and Approximate Design: Retrospects and Prospects.
Krishna V. Palem, Lakshmi N.B. Chakrapani, Zvi M. Kedem, Avinash Lingamneni and Kirthi Krishna Muntimadugu

1.2 Complete Nanowire Crossbar Framework Optimized for the Multi-Space Patterning Technique.
M. Haykel Ben-Jamaa, Gianfranco Cerofolini, Yusuf Leblebici and Giovanni De Micheli

1.3 III-V/Si Integration: Potential and Outlook for Integrated Low Power Micro and Nanosystems.
Soon Fatt Yoon

SESSION 1A: FRAMEWORKS FOR PLATFORM MODELING AND EXPLORATION
Session chair: Christian Haubelt
Session co-chair: Andreas Gerstlauer

1.1 A Compositional Modeling Framework for Exploring MPSoC Systems.
Anders Sejer Tranberg-Hansen and Jan Madsen

1.2 A High-Level Virtual Platform for Early MPSoC Software Development.
Jianjiang Ceng, Weihua Sheng, Jeronimo Castrillon, Anastasia Stulova, Rainer Leupers, Gerd Ascheid and Heinrich Meyr

1.3 Portable SystemC-on-a-chip.
Scott Sirowy, Bailey Miller and Frank Vahid

SESSION 1B: TOOLS FOR EMBEDDED SOFTWARE DESIGN
Session chair: Tony Givargis
Session co-chair:...

Sjoerd Meijer, Hristo Nikolov and Todor Stefanov

1.2 SARA: Stream Register Allocation.
Praveen Raghavan and Francky Catthoor

1.3 Dynamically Utilizing Computation Accelerators for Extensible Processors in a Software Approach.
Yashuai Lv, Li Shen, Zhiying Wang and Nong Xiao

SESSION 1: ENERGY AWARE DESIGN
Session chair: Petru Eles

1.1 Aggressive Dynamic Voltage Scaling for Energy-Aware Video Playback Based on Decoding Time Estimation.
Ahron Yang and Minseok Song

1.2 Markov Decision Process (MDP) Framework for Optimizing Software on Mobile Phones.
Tang Lung Cheung, Kari Okamoto, Xin Liu, Frank Maker and Venkatesh Akella

Andrea Bartolini, Martino Ruggiero and Luca Benini

SESSION 2: COMPILER TECHNIQUES FOR PERFORMANCE
Session chair: Laura Pozzi
Session co-chair: Lakshmi Chakrapani

2.1 Exploiting Residue Number System for Power-Efficient Digital Signal Processing in Embedded Processors.
Rooju Chokshi, Krzysztof Berezowski and Aviral Shrivastava

2.2 Fast Enumeration of Maximal Valid Subgraphs for Custom-instruction Identification.
Tao Li, Zhigang Sun, Wu Jigang and Xicheng Lu

2.3 Hybrid Multithreading for VLIW Processors.
Manoj Gupta, Josep Llosa and Fermín Sánchez

2.4 Spatial Complexity of Reversibly Computable DAGs.
Mouad Bahi and Christine Eisenbeis

SESSION 2A: SYSTEM LEVEL MODELING AND SIMULATION
Session chair: Franco Fummi
Session co-chair: Adrien Boscotti and Sandeep Kulkarni

2.1 Compositional Verification of Real-Time Fault-Tolerant Programs.
Borooz Bonadarpour and Sandeep Kulkarni

2.2 Compositional Timing Analysis.
Ramzi Ben Salah, Marius Boega and Oded Maler

2.3 Refining the Control Structure of Loops using Static Analysis.
Gogul Balakrishnan, Srijan Sankaranarayanan, Franjo Ivancic and Aarti Gupta

2.4 Compositional Deadlock Detection for Rendezvous Communication.
Babir Shao, Nalini Vasudevan and Stephen Edwards

SESSION 2B: ARCHITECTURE AND ROUTING FOR NOC
Session chair: Karam Chattha
Session co-chair: Zhonghai Lu

2.1 An On-Chip Interconnect and Protocol Stack for Multi-Processor Systems.
Andreas Hansson and Kees Goossens

2.2 A monitoring and adaptive routing mechanism for QoS traffic on mesh NoC architectures.
Leonel Tedesco, Fabien Clermidy and Fernando Moraes

2.3 A DP-Network for Emergent Chip Multiprocessors.
Shirish Bahirat and Sudeep Pasricha

ESWEEK 2009
October 12, Monday 10:00 - 12:30
EMSOFT + ISSS
POSTER SESSION @ 12:00